

METHOD, APPARATUS, AND COMPUTER PROGRAM PRODUCT
FOR CONTENTION TESTING

BACKGROUND

5 **Field of the Invention**

This invention relates generally to testing of designs for integrated circuits, and more particularly to testing for contention among drivers in such designs.

Related Art

10 With modern technology, a tiny integrated circuit having a huge number of transistors can be fabricated in large quantities at a relatively small per unit cost. However, in absolute terms the set up cost for fabrication is not cheap. To achieve low per unit cost integrated circuit chips must be produced in large quantities. Because it is expensive to set up fabrication, and because chips having perhaps millions of transistors are complicated and subject to design glitches, it is
15 common to emulate a chip and extensively test the emulated chip before fabrication.

It is also quite common for chips to interface with one another. In this circumstance, testing is not as simple as just testing a single chip's functionality. Interaction between the chips must also be tested. But even with extensive conventional testing, chips may appear to interact properly and yet have undetected problems.

20 One commonly undetected problem concerns contention between drivers. This occurs when two drivers that share a transmission line or node both drive at the same time. It is particularly problematic to detect contention because when two drivers contend, one of the drivers typically overpowers the other. This may result in correct logic functioning due to the

happenstance of which of the drivers happens to win. However, while correct logic functioning is good, it is not all that matters. Contention that does not impair logic function is still undesirable because it causes unnecessary noise and power dissipation. Moreover, even contention that does not initially impair logic function may lead to incorrect functioning later.

- 5 For example, logic designs for chips may be somewhat independent of drivers. Thus, in one instance chips may have their logics fabricated with one type of drivers, in which case the chips interact successfully, but in another instance the chips may have a different type of drivers and no longer function properly together. Therefore, a need exists for improvements in testing for contention.

SUMMARY

The foregoing need is addressed in the present invention. In one aspect of the invention, a method for testing includes interposing a tester between first and second logic. The first logic and second logic have respective first and second output drivers. The tester operates in test
5 cycles to detect dynamic contention responsive to a signal asserted by the first driver during one of the test cycles and a signal asserted by the second driver during an immediately succeeding one of the test cycles. Static contention is detected responsive to a signal asserted by the first driver during one of the test cycles and a signal asserted by the second driver during the same one of the test cycles.

10 In an apparatus form, a tester is for interposing between first and second logic. The first logic and second logic have respective first and second output drivers and the tester is operable in test cycles to periodically test for contention between the drivers. The tester has tester logic, a first tester node for coupling to the first logic driver, and a second tester node for coupling to the second logic driver. A switch of the tester is coupled to the first and second tester nodes, and the
15 tester logic is operatively coupled to the switch to open the switch during a certain interval of the test periods, so that the respective first and second logic may be electrically decoupled from one another. A first test receiver is coupled to the first tester node and to the tester logic for sensing a signal on the first node. Likewise, a second test receiver is coupled to the tester second node and to the tester logic for sensing a signal on the second node. The periodic testing for contention
20 includes signals of the logic output drivers during the certain interval being registered by the tester logic responsive to the respective test receivers.

In another aspect, the tester has a first test source coupled to the first tester node for asserting and de-asserting signals on the first node during one portion of the certain interval

responsive to the tester logic, and a second test source coupled to the second tester node for asserting and de-asserting signals on the second node during another portion of the certain interval, also responsive to the tester logic. The test receivers sense the logic driver signals during the certain interval responsive to the test source signals.

- 5 Other aspects, as well as advantages and objects of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a test arrangement, according to an embodiment of the present invention.

FIG. 2 illustrates certain aspects of the tester and devices under test, according to an embodiment of the present invention.

FIG. 3 illustrates certain timing aspects of testing, according to an embodiment of the present invention.

FIG. 4 illustrates certain aspects of detecting dynamic contention, according to an embodiment of the present invention.

FIG. 5 illustrates certain aspects of detecting static contention, according to an embodiment of the present invention.

FIG. 6 illustrates certain method steps of the testing, according to an embodiment of the present invention.

FIG. 7 illustrates certain additional method steps of the testing, according to an embodiment of the present invention.

FIG. 8 illustrates, in a state diagram form, certain aspects of detecting static and dynamic contention, according to an embodiment of the present invention.

DETAILED DESCRIPTION

The claims at the end of this application set out novel features which applicants believe are characteristic of the invention. The invention, a preferred mode of use, further objectives and advantages, will best be understood by reference to the following detailed description of an illustrative embodiment read in conjunction with the accompanying drawings.

Referring now to FIG. 1, a test arrangement is illustrated, according to an embodiment of the present invention. In the illustrated embodiment, a bus bridge 120 under development and testing goes between a central processing unit ("CPU") 110 and a memory 130. As illustrated, a tester 140 is interposed on bus 115 between the bridge 120 and CPU 110, for testing aspects of operation of the bridge 120 which relate to the CPU 110.

In the illustrated testing arrangement, the CPU 110 and memory 130 are actual, very large scale integrated circuitry ("VLSI") parts, which have respective specified operating frequencies. For example, in an embodiment, the CPU 110 is specified for operation at 1000 MHz, while the memory 130 has a specified operating frequency of 200 MHz. Likewise, the bus bridge 120 has a specified operating frequency, which, in an embodiment, corresponds to that of the memory 130, that is, 200 MHz.

In the arrangement illustrated, an emulated version of the bridge 120 is being tested. That is, the bridge 120 is not yet fabricated as one or more VLSI parts. Rather, the bridge 120 as shown in FIG. 1 is instantiated in one or more field programmable gate arrays ("FPGA's") as a representation of the final part. In another embodiment, the bridge 120 is emulated for the most part by a software program representing logic of the bridge 120. In this alternative sort of emulation, the software program representing the logic runs on a computer system, or more typically on numerous computer systems running concurrently, and actual hardware drivers for

the bridge 120 interface to the program so that the functioning of the emulated bridge 120 can be tested with respect to external parts, that is, memory 130 and CPU 110.

Neither the FPGA emulation of the bridge 120, nor the software emulation are capable of operating at the specified frequency for the finally fabricated bridge. The emulation in which the logic of the bridge 120 is represented by software is capable of operating at only a very low frequency, depending upon a number of factors, such as the computing resources available. In a typical test run, a software emulation may require hours of run time to emulate a single cycle of bridge 120 operation. The FPGA emulation is capable of operating at a frequency that is much faster than the software emulation. In an embodiment, the FPGA emulated bridge 120 is capable of operating at a frequency of 2 MHz.

For testing with the emulated bridge 120, the CPU 110 and memory 130 are operated at the bridge 120 emulation testing frequency, such as 2 MHz for the FPGA emulation, and not at their specified, normal operating frequencies. Ordinarily, the specified operating frequency for a memory and bridge is limited by timing issues that concern reliably driving signals onto an interconnecting bus and capturing signals from the bus. Thus, in this testing circumstance, the non-emulated devices are being operated at a much lower frequency than their capabilities would permit. Consequently, a great deal of the time during a test cycle is not needed or used for driving, transmitting or capturing signals on the bus. This gives rise to an opportunity to use the otherwise unused time in a test cycle to perform additional analysis. The unused time in the present embodiment is used to test for contention among drivers.

Referring now to FIG. 2, details are shown of aspects of the tester 140, CPU 110 and bridge 120 of FIG. 1. The tester 140 has a first tester node 252 connected to a portion of bus 115 that terminates at terminating resistor RT2 on CPU 110, and a second tester node 254 connected

to another portion of bus 115 that terminates at terminating resistor RT1 on bridge 120. The illustrated portion of CPU 110 has a receiver 214 coupled to a terminating resistor RT2 for receiving signals from the bus 115, and driver 216 synchronized by a clock 205 for driving signals on the terminating resistor RT2 and bus 115. It should be understood that CPU portion

5 212 includes other receivers and drivers, as well as CPU 110 logic, memory registers, etc. Likewise, the illustrated portion of bridge 120 has a receiver 224 coupled to a terminating resistor RT1 for receiving signals from the bus 115, and a driver 226 synchronized by clock 205 for driving signals on the terminating resistor RT1 and bus 115. Similarly, it should be understood that bus bridge portion 222 includes other receivers and drivers, logic, memory

10 registers, etc.

Interconnecting the first tester node 252 and second tester node 254 is an electronic switch 242 operatively coupled to tester logic 250, which opens and closes responsive to the tester logic 250, in order to decouple and couple the portions of bus 115, and, correspondingly, CPU 110 and bridge 120. The tester 140 also has a first current source 242 coupled to the first

15 tester node 252 and a second current source 244 coupled to the second node 254. The current sources 242 and 244 are operatively coupled to tester logic 250 to drive signals on to the nodes 252 and 254, responsive to tester logic 250. The tester 140 also has a first receiver 246 and a second receiver 248 coupled to the respective nodes 252 and 254 and operatively coupled to the tester logic 250 for sensing signals on the nodes, responsive to the tester logic 250. The tester

20 logic 250 also receives clock 205, which operates at the emulation testing frequency for synchronizing the testing.

Referring now to FIG. 3, certain timing aspects of the operation of tester 140, CPU 110 and bridge 120 are illustrated for one test cycle of clock 205, according to an embodiment.

During the first three-quarters of the cycle, that is, interval 350 from time t0 to time t3, tester logic 250 opens switch 242 of tester 140 (FIG. 2), so that any signals driven onto the bus 115 by drivers 216 and 226 are *not* transferred between CPU 110 and bridge 120 during this interval 350. During the last quarter of the cycle, that is, interval 360 from time t3 to time t0 of the next cycle, tester logic 250 closes the switch 242, so that any signals driven onto the bus 115 by drivers 216 and 226 *are* transferred between CPU 110 and bridge 120 during this interval.

During a first portion of the first interval 350, that is, interval 310 from time t0 to time t1, tester 140 waits to give drivers 216 and 226 time to turn on or off and thereby drive signals onto the bus 115. Then, during the next portion of the first interval 350, that is interval 320 from time t1 to time t2, tester logic 250 causes current sources 242 and 244 to attempt to drive logical "1" signals on the bus 115, and causes receivers 246 and 248 to sense the respective node 252 and 254 voltages. Then, during the next portion of the first interval 350, that is interval 330 from time t2 to time t3, tester logic 250 causes current sources 242 and 244 to attempt to drive logical "0" signals on the bus 115, and causes receivers 246 and 248 to again sense the respective node 252 and 254 voltages.

The voltages sensed by receivers 246 and 248 responsive to signals driven by current sources 242 and 244 depend upon the states of drivers 216 and 226. That is, for example, if driver 216 is not actively driving a signal during the test cycle, then the tester node 252 voltage will follow the signal driven by current source 242. In this case, during interval 320 receiver 246 will sense that node 252 is high,. Then, during interval 330 receiver 246 will sense that node 252 is low and this will be registered by tester logic 250. On the other hand, current source 242 is intentionally designed such that if a driver 216 is actively driving during the cycle, then the driver 216 signal will overpower the current source 242 signal, so that during both intervals 320

and 330 the same signal, i.e., whatever signal the driver 216 is driving, will be sensed by receivers 246 and registered by tester logic 250. After registering the signals sensed in intervals 320 and 330 on node 252, for example, tester logic 250 compares the signals and determines whether driver 216 is active or not.

5 Referring now to FIG. 4, certain aspects are illustrated concerning how tester logic 250 detects dynamic contention between drivers 216 and 226 responsive to the signals driven by sources 242 and 244, sensed by receivers 248 and 246, and registered by test logic 250. In the example illustrated, driver 226 is active during test cycle N, and turns off responsive to the rising edge of clock 205 in cycle N+1. Driver 216 is not active during test cycle N, but turns on responsive to the rising edge of clock 205 in cycle N+1. Tester logic 250 detects dynamic (a.k.a. "transient") contention responsive to registering that driver 226 was active in cycle N but not in cycle N+1, and that driver 216 was not active in cycle N, but was active in cycle N+1.

10 Referring now to FIG. 5, certain aspects are illustrated concerning how tester logic 250 detects static contention between drivers 216 and 226 responsive to the signals driven by sources 242 and 244, sensed by receivers 248 and 246, and registered by test logic 250. In the example illustrated, driver 226 is active during both test cycles N and N+1, and turns off responsive to the rising edge of clock 205 in cycle N+2. Driver 216 is not active during test cycle N, but turns on responsive to the rising edge of clock 205 in cycle N+1. Tester logic 250 detects static contention responsive to registering that drivers 216 and 226 are both active in cycle N+1.

15 Referring now to FIG. 6, certain method aspects of a test cycle are illustrated, according to an embodiment. Beginning after 605, devices that are being tested, such as CPU 110 and bridge 120 in FIG. 1, are decouple from one another at 610 by the tester. Next, at 615, the tester waits for drivers in the devices being tested to begin driving signals. Then, at 620, the tester

detects driver signals for an interval. Next, at 625, before the end of the cycle the tester recouples the devices being tested to permit data to transfer between them. Concurrently, at 630, logic in the tester analyzes the driver signals that were detected in order to check for contention. The method steps for FIG. 6 then end at 635.

5 Referring now to FIG. 7, further details are illustrated concerning step 620 in FIG. 6, according to an embodiment. After beginning at 705, a logic level "1" signal is sourced on a node of the tester at 710 for an interval during the test cycle. Next, at 715, the effect of the signal on the tester node is sensed and registered by the tester. Then, at 720, in logic level "0" signal is sourced by the tester for a next interval, and the effect of the signal is sensed and registered at
10 step 725.

Next, at 730, the tester logic compares the registered states of the tester node in the two intervals to determine an implied state of the driver of the device under test. If the same signal is sensed on the node in both intervals, this means that the driver of the device under test was active and overpowered the signals sourced by the tester, and at 735 an indication is returned to that
15 effect. If the different signals are sensed on the node in the two intervals, this means that the driver of the device under test was not active and the two different signals sourced by the tester drove the node to two respectively different states, and at 740 an indication is returned to that effect. The detection steps of FIG. 7 then end at 745.

Referring now to FIG. 8, further details are illustrated in the form of a state diagram
20 concerning step 630 in FIG. 6, according to an embodiment. In the state diagram of FIG. 8 the states 805, 810, 815 and 820 indicate the states during a test cycle of two drivers under test, such as driver 216 and driver 226. In FIG. 8, "A" indicates an active driver, and "N_A" indicates an inactive driver. Dynamic contention is detected in comparing driver states in successive cycles,

and therefore is represented in the state diagram as arising from transitions among the states 805, 810, 815 and 820. As shown, dynamic contention arises from a transition from state 815 to state 820 or vice versa, where in a first state one of the drivers is active and the other is inactive, and in a next state the previously active driver becomes inactive and the previously inactive driver becomes active. In contrast to dynamic contention, static contention arises during a single cycle when both drivers are active, i.e., state 805. Therefore, state 805 itself indicates static contention, and any transition to or from state 805 is not meaningful ("N.M.").

The description of the present embodiment has been presented for purposes of illustration, but is not intended to be exhaustive or to limit the invention to the form disclosed. Many additional aspects, modifications and variations are also contemplated and are intended to be encompassed within the scope of the following claims. For example, it is important to note that while the present invention has been described primarily in the context of a hardware implementation, those of ordinary skill in the art will appreciate that at least certain aspects of the tester 140, particularly the tester logic 250 may be implemented as a fully functioning data processing system. Furthermore, processes of the present invention are capable of being distributed in the form of a computer readable medium of instructions in a variety of forms. The present invention applies equally regardless of the particular type of signal bearing media actually used to carry out the distribution. Examples of computer readable media include RAM, flash memory, recordable-type media, such a floppy disk, a hard disk drive, a ROM, and CD-ROM, and transmission-type media such as digital and analog communications links, e.g., the Internet.

It should also be understood that the tester described herein may be applied in a variety of contexts. For example, the tester 140 of FIG. 1 may also be interposed on bus 125 between the

bridge 120 and the memory 130 in a subsequent test, or even during a test concurrent to the test of the functioning of the bridge 120 with the CPU 110. More generally, the tester may be interposed between logics having drivers that share a node or conductor irrespective of the nature of the logics.